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**DOCKET NO. STMI07-02021**
**CUSTOMER NO. 23990**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | |
|---|---|---|
| In re application of | : | Franck Badets, et al. |
| Serial No. | : | 10/603,579 |
| Filed | : | June 25, 2003 |
| For | : | VARIABLE PHASE-SHIFTING CIRCUIT, PHASE INTERPOLATOR INCORPORATING IT, AND DIGITAL FREQUENCY SYNTHESIZER INCORPORATING SUCH AN INTERPOLATOR |
| Group No. | : | 2816 |
| Examiner | : | Tuan Thieu Lam |
| Confirmation No. | : | 4869 |

**MAIL STOP APPEAL BRIEF - PATENTS**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**CERTIFICATE OF MAILING BY FIRST CLASS MAIL**

Sir:

The undersigned hereby certifies that the following documents:

1. Appeal Brief Under 37 C.F.R. § 41.37
2. Check in the amount of $540.00 for Appeal Brief fee;
3. Fee transmittal for FY 2009; and
4. A postcard receipt

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on **January 12, 2009**.

Date: January 12, 2009

Mailer

Date: January 12, 2009

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


*Effective on 12/08/2004.*
*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).*

# FEE TRANSMITTAL For FY 2009



☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) $540.00

| Complete if Known | |
|---|---|
| Application Number | 10/603,579 |
| Filing Date | June 25, 2003 |
| First Named Inventor | Franck Badets |
| Examiner Name | Tuan Thieu Lam |
| Art Unit | 2816 |
| Attorney Docket No. | STMI07-02021 |

## METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0208 Deposit Account Name: Munck Carter, P.C.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

## FEE CALCULATION

### 1. BASIC FILING, SEARCH, AND EXAMINATION FEES

| Application Type | FILING FEES Fee ($) | FILING FEES Small Entity Fee ($) | SEARCH FEES Fee ($) | SEARCH FEES Small Entity Fee ($) | EXAMINATION FEES Fee ($) | EXAMINATION FEES Small Entity Fee ($) | Fees Paid ($) |
|---|---|---|---|---|---|---|---|
| Utility | 330 | 165 | 540 | 270 | 220 | 110 | |
| Design | 220 | 110 | 100 | 50 | 140 | 70 | |
| Plant | 220 | 110 | 330 | 165 | 170 | 85 | |
| Reissue | 330 | 165 | 540 | 270 | 650 | 325 | |
| Provisional | 220 | 110 | 0 | 0 | 0 | 0 | |

### 2. EXCESS CLAIM FEES

| Fee Description | Fee ($) | Small Entity Fee ($) |
|---|---|---|
| Each claim over 20 (including Reissues) | 52 | 26 |
| Each independent claim over 3 (including Reissues) | 220 | 110 |
| Multiple dependent claims | 390 | 195 |

| Total Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - 20 or HP = | _____ | x _____ | = _____ |

HP = highest number of total claims paid for, if greater than 20.

| Indep. Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - 3 or HP = | _____ | x _____ | = _____ |

HP = highest number of independent claims paid for, if greater than 3.

| Multiple Dependent Claims Fee ($) | Multiple Dependent Claims Fee Paid ($) |
|---|---|
| _____ | _____ |

### 3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | Extra Sheets | Number of each additional 50 or fraction thereof | Fee ($) | Fee Paid ($) |
|---|---|---|---|---|
| _____ - 100 = | _____ | / 50 = _____ (round up to a whole number) | x _____ | = _____ |

### 4. OTHER FEE(S)

| | Fees Paid ($) |
|---|---|
| Non-English Specification, $130 fee (no small entity discount) | |
| Other (e.g., late filing surcharge): Appeal Brief fee | $540.00 |

## SUBMITTED BY

| | | | |
|---|---|---|---|
| Signature | | Registration No. (Attorney/Agent) 39,308 | Telephone 972-628-3600 |
| Name (Print/Type) | William A. Munck | | Date 1-12-09 |

**DOCKET NO. STMI07-02021** **PATENT**
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## APPEAL BRIEF UNDER 37 C.F.R. § 41.37

This Appeal Brief Under 37 C.F.R. § 41.37 ("Appeal Brief") is filed in furtherance of a Notice of Appeal and a Pre-Appeal Brief Request for Review that were mailed on November 5, 2008. A Notice of Panel Decision from Pre-Appeal Brief Review was mailed to the Appellants on December 12, 2008. Therefore, the due date for filing this Appeal Brief is January 12, 2009.

01/15/2009 NNGUYEN1 00000011 10603579
01 FC:1402 540.00 OP

**Real Party in Interest** **37 C.F.R. § 41.37 (c)(1)(i)**

This patent application is currently owned by STMicroelectronics, S.A., a corporation having a place of business at 29 Boulevard Romain Rolland, 92120 Montrouge, France. The Assignment from the inventors to STMicroelectronics, S.A. was recorded in the Patent and Trademark Office on November 7, 2003 on Reel 014671 and Frame 0606.

**Related Appeals or Interferences** **37 C.F.R. § 41.37 (c)(1)(ii)**

None. There are no appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

**Status of Claims** **37 C.F.R. § 41.37 (c)(1)(iii)**

Claims 1-2, 24-29 and 33-36 have been rejected in a final Office Action that was mailed on August 5, 2008.

Claims 3, 30-32 and 37-39 have been objected to.

Claims 4-23 have been withdrawn due to a restriction requirement.

Claims 1-2, 24-29 and 33-36 are presented for appeal.

A copy of the claims involved in the appeal is provided in Appendix A.

**Status of Amendments after Final** **37 C.F.R. § 41.37 (c)(1)(iv)**

1. The Appellants filed a RESPONSE UNDER 37 C.F.R. § 1.116 on September 16, 2008 and requested reconsideration of the claim rejections and requested an Advisory Action.

2. The Examiner issued an Advisory Action on September 29, 2008 but continued the rejections of Claims 1-2, 24-29 and 33-36.

3. The Appellants filed a PRE-APPEAL BRIEF REQUEST FOR REVIEW on November 5, 2008 and requested reconsideration of the claim rejections.

4. The Panel issued a Notice of Panel Decision from Pre-Appeal Brief Review on December 12, 2008 but continued the rejections of Claims 1-2, 24-29 and 33-36.

5. No amendments to the claims have been submitted and refused entry after issuance of the final Office Action dated August 5, 2008.

**Summary of Claimed Subject Matter** **37 C.F.R. § 41.37 (c)(1)(v)**

*The following general discussion provides background for understanding the invention. A concise explanation of the subject matter of the invention defined in each of the independent claims involved in the appeal is set forth below after the general discussion.*

**General Discussion**

The present invention generally relates to the field of digital frequency synthesis. More specifically, the present invention discloses (1) a variable phase shifting circuit, and (2) a phase interpolator that incorporates the variable phase shifting circuit, and (3) a digital frequency synthesizer that incorporates the phase interpolator. (Specification, Page 1). Claims directed to the phase interpolator (Claims 4-13) and claims directed to the digital frequency synthesizer (Claims 14-23) have been previously withdrawn due to a restriction requirement. Claims 1-3 and Claims 24-39 are directed to the variable phase shifting circuit.

An oscillator is a circuit that includes self-oscillating means and an output for generating an oscillating signal. (Specification, Page 5, Lines 32-33). An oscillator is characterized by a free-running frequency (designated $F_O$) which is normally the output signal frequency. (Specification, Page 5, Line 33 to Page 6, Line 2). All oscillators have the property of copying the frequency of an interfering signal if it is close to the free-running oscillation frequency $F_O$ of the oscillator. (Specification, Page 6, Lines 3-5). All oscillators are characterized by a synchronization range whose width depends on the amplitude of the interfering signal and the topology of the oscillator. (Specification, Page 6, Lines 5-7). Knowing the amplitude of the

interfering signal (called the synchronization signal), it is possible to calculate the synchronization range (designated $\Delta F$) of the oscillator based on calculating the oscillator's elasticity factors. (Specification, Page 6, Lines 7-10).

A synchronized prior art oscillator (designated OS) is shown in FIGURE 1 of the patent application. The synchronized oscillator OS includes an input (designated In) for receiving a synchronization signal (designated Sin) and an output (designated Out) for delivering an output signal (designated Sout). (Specification, Page 6, Lines 15-17). The free-running frequency of the oscillator OS is denoted by $F_O$, the synchronization signal frequency is denoted by Fin, and the output signal frequency is denoted by Fout. (Specification, Page 6, Lines 17-19).

The change in the frequency Fout as a function of the frequency Fin is illustrated in the graph that is shown in FIGURE 2 of the patent application. The frequency Fout is equal to frequency $F_O$ for values of Fin that are outside of the synchronization range $\Delta F$ that is centered on the value $F_O$. (Specification, Page 6, Lines 20-23). For values of Fin inside the synchronization range $\Delta F$, the value of Fout is equal to Fin. (Specification, Page 6, Lines 23-24).

When the oscillator is synchronized, the difference in phase (designated $\Delta\varphi$) between the synchronization signal Sin and the oscillator signal output signal Sout is only a function of Fin, Fout and $\Delta F$. (Specification, Page 6, Lines 28-30). In conventional applications of prior art synchronized oscillators, the input value is the synchronization signal frequency Sin. (Specification, Page 7, Lines 3-4).

In the variable phase shifting circuit of the invention, the value of the synchronization signal frequency Sin is left fixed and the free-running oscillation frequency $F_O$ of the oscillator is altered like a controlled oscillator. (Specification, Page 7, Lines 4-6). The variation in frequency $F_O$ is limited so that the frequency Fin remains within the resultant synchronization range SF of the oscillator. Thus the frequency Fout is equal to Fin (Specification, Page 7, Lines 6-9). The phase shift $\Delta\varphi$ of the oscillator output signal is controlled with respect to the synchronization signal. (Specification, Page 7, Lines 11-12).

The variable phase shifting circuit of the invention comprises a synchronized oscillator and a control input that receives a control signal whose function it is to vary the phase shift $\Delta\varphi$ between the output signal and the input signal of the synchronized oscillator by varying the free-running oscillation frequency $F_O$ of the oscillator. (Specification, Page 7, Lines 12-16).

The variable phase shifting circuit of the invention comprises (1) an input for receiving an input signal with a specified oscillation frequency, and (2) an output for delivering an output signal having the specified oscillation frequency and having a variable phase shift with respect to the input signal, and (3) at least one control input for receiving a control signal that controls the phase shift. (Specification, Page 2, Line 31 to Page 3, Line 3). The variable phase shifting circuit of the invention comprises a synchronized oscillator having at least one synchronization input coupled to the input of the variable phase shifting circuit for receiving the input signal, and at least one output coupled to the output of the variable phase shifting circuit for delivering the output signal. (Specification, Page 3, Lines 3-7). The synchronized oscillator has a variable

free-running oscillation frequency that is controlled by the control signal. (Specification, Page 3, Lines 7-9).

**Support for Independent Claims** **37 C.F.R. § 41.37 (c)(1)(v)**

*Note that, per 37 C.F.R. § 41.37, only the independent claims are discussed in this section. The discussion of the claims in this section is for illustrative purposes and is not intended to affect the scope of the claims.*

A schematic representation of an exemplary embodiment of a variable phase-shifting circuit of the invention is shown in FIGURE 4 of the patent application. A detailed diagram of an exemplary embodiment of the variable phase-shifting circuit of the invention is shown in FIGURE 5 of the patent application.

Claim 1 is directed to a variable phase-shifting circuit 40 that comprises (1) an input (designated A) for receiving an input signal (Sin) having a specified oscillation frequency, and (2) an output (designated B) for delivering an output signal (designated Sout) having the specified oscillation frequency and having a variable phase-shift (designated $\Delta\varphi$) with respect to said input signal, and (3) at least one control input (designated C) for receiving a control signal (designated Is) which controls the phase-shift ($\Delta\varphi$) of the output signal (Sout) with respect to the input signal (Sin). (Specification, Figure 4, Page 7, Lines 17-23).

The variable phase-shifting circuit 40 comprises a synchronized oscillator (100, 111, 112) that is coupled to the output (B) of the variable phase-shifting circuit 40 in which the synchronized oscillator (100, 111, 112) has a variable free-running oscillation frequency (designated $F_O$) that is controlled by the control signal (Is) wherein the input signal (Sin)

originates from a source that is external to the synchronized oscillator (100, 111, 112). (Specification, Figure 5, Page 7, Line 24 to Page 9, Line 28).

Claim 4 and Claim 14 have been withdrawn due to a restriction requirement.

Claim 24 is directed to a variable phase-shifting circuit 40 that comprises an input (A) and an output (B) having a specified oscillation frequency, wherein the output (B) has a variable phase-shift ($\Delta\varphi$) with respect to the input (A), and a control signal (Is) for controlling the phase-shift ($\Delta\varphi$) of the output (B) with respect to the input (A). The variable phase-shifting circuit 40 comprises a synchronized oscillator (100, 111, 112) having a synchronization input coupled to the input (A) of the variable phase-shifting circuit 40 and a second output coupled to the output (B) of the variable phase-shifting circuit 40, wherein the synchronized oscillator (100, 111, 112) has a variable free-running oscillation frequency ($F_O$) that is controlled by the control signal (Is) and wherein the input (A) of the variable phase-shifting circuit 40 originates from a source that is external to the synchronized oscillator (100, 111, 112). (Specification, Figure 5, Page 7, Line 24 to Page 9, Line 28).

Claim 33 is directed to a variable phase-shifting circuit 40 that comprises an input (A) and an output (B) having a specified oscillation frequency, wherein the output (B) has a variable phase-shift ($\Delta\varphi$) with respect to the input (A), and a control signal (Is) originating from a source external to the variable phase-shifting circuit 40 to control the phase-shift ($\Delta\varphi$) of the output (B) with respect to the input (A), and a synchronized oscillator (100, 111, 112) having a synchronization input coupled to the input (A) of the variable phase-shifting circuit 40 and a

second output coupled to the output (B) of the variable phase-shifting circuit 40, wherein the synchronized oscillator (100, 111, 112) has a variable free-running oscillation frequency ($F_O$) controlled by the control signal (Is), and wherein the synchronized oscillator (100, 111, 112) comprises an astable multivibrator circuit (100) having a first branch (101) and a second branch (102) arranged in parallel between a positive supply terminal (10) and a negative supply terminal or ground (Gnd) of said variable phase-shifting circuit 40. (Specification, Figure 5, Page 7, Line 24 to Page 9, Line 28).

**Grounds of Rejection to be Reviewed on Appeal** **37 C.F.R. § 41.37 (c)(1)(vi)**

1. Claims 1-2, 24-29 and 33-36 were rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent No. 6,469,585 issued to Liang Dai et al. ("*Dai*").

**Argument** **37 C.F.R. § 41.37 (c)(1)(vii)**

**Stated Grounds of Rejection for Claims 1-2, 24-29 and 33-36**

Ground of Rejection 1: Claims 1-2, 24-29 and 33-36 are rejected under § 102(e) as being anticipated by United States Patent No. 6,469,585 issued to Liang Dai et al. ("*Dai*").

**Legal Standard for Anticipation**

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131. *See*, *In re King*, 231 USPQ 126, 138 (Fed. Cir. 1986) (citing with approval, *Lindemann Maschinenfabrik v. American Hoist and Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984)); *In re Bond*, 910 F.2d 831, 832, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131. *In re Donohue*, 766 F.2d 531, 534, 226 USPQ 619, 621 (Fed. Cir. 1985).

With respect to any of Claims 1-2, 24-29 and 33-36, a determination of anticipation in accordance with Section 102 requires that each feature claimed therein be described in sufficient detail in the *Dai* reference to enable one of ordinary skill in the art to make and practice the claimed invention.

**Analysis of Examiner's Rejections**

The cited references are briefly discussed in relevant part for the appropriate rejections, and each rejection is addressed separately below.

**Ground of Rejection 1: Claims 1-2, 24-29 and 33-36 are rejected under § 102(e) as anticipated by U.S. Patent No. 6,469,585 issued to Dai et al. ("*Dai*").**

On Pages 2-3 of the August 5, 2008 Office Action, the Examiner rejected Claims 1-2, 24-29 and 33-36 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,469,585 to Liang Dai et al. ("*Dai*"). The Appellants respectfully traverse these rejections for the reasons set forth below.

The Examiner stated that the circuit shown in Figure 3 of the *Dai* reference anticipates the Appellants' invention as claimed in Claims 1-2, 24-29 and 33-36. (August 5, 2008 Office Action, Pages 2-3). The Appellants respectfully point out that the circuit that is shown in Figure 3 of the *Dai* reference is a delay stage 32 for a ring-type voltage controlled oscillator 30. The delay stage 32 comprises inverters (33 and 34), a memory circuit (35) and tuning circuitry (transistors M1, M4, M7 and M10). The transistors of the tuning circuitry function as variable resistors to tune the amount of delay of the delay stage 32, and hence the frequency of the voltage controlled oscillator 30. (*Dai*, Column 4, Lines 23-28). The frequency (not the phase) is tuned. Therefore, the *Dai* reference does not show a phase shifter circuit.

The *Dai* reference states that each delay stage (32A and 32B) causes a ninety degree phase shift. The *Dai* reference states "Each delay stage 32A and 32B causes a 90° phase shift, and so the phase shifts relative to $V_{OUT+}$ of delay stage 32A are as follows – $V_{OUT+}$ of delay stage 32A is shifted 90°, $V_{OUT-}$ of delay stage 32A is shifted 180°, and $V_{OUT-}$ of delay stage 32B is shift[ed] 270°." (*Dai*, Column 3, Lines 54-59).

It is clear that the *Dai* delay stages (32A and 32B) each cause a fixed phase shift of 90°. The value of phase shift is 90° is a fixed value and is not a variable value. Therefore, the delay stages (32A and 32B) of the *Dai* reference are not "variable phase shifting circuits." Because the claims of the Appellants' patent application require a variable phase shifting circuit (and not a fixed phase shifting circuit), the *Dai* reference does not anticipate the Appellants' invention.

The Examiner stated that the transistors M1 and M7 and the cross coupled transistors M5 and M6 in the *Dai* reference form a synchronized oscillator that maintain an oscillation of the output signal. (August 5, 2008 Office Action, Page 2, Lines 21-23). The Appellants respectfully traverse this assertion of the Examiner. The *Dai* reference states that "The memory element 35 in the configuration shown in FIG. 3 operates to prevent the outputs of inverters 33 and 34 from switching states when they otherwise would switch. In other words, memory element 35 causes switching to be delayed." (*Dai*, Column 5, Lines 58-62). The Appellants respectfully submit that the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

The cross coupled transistors M5 and M6 constitute a very stable circuit 35 (as it must be for a memory, namely a latch). The electrical state of this memory circuit 35 can only be changed by applying a switching signal at the input. In the absence of such switching signal input to the cross coupled transistors M5 and M6, there will be no variation at the output. Therefore, the memory circuit 35 can not be equivalent to an oscillator circuit.

Furthermore, the *Dai* reference states that "In accordance with the invention, the strength of inverters 33 and 34 is variable and dependent upon the control voltage received by the tuning transistors M1, M4, M7 and M10, whereas the strength of the memory element 35 remains relatively constant as it is tied, in the case of FIG. 3, to the power supply voltage $V_{DD}$." (*Dai*, Column 5, Line 67 to Column 6, Line 6) (Emphasis added). Because the strength of the memory element 35 remains relatively constant, the memory element 35 is not a synchronized oscillator that has a variable free-running oscillation frequency that is controlled by a control signal. There is no control signal in the *Dai* reference that controls the relatively constant memory element 35. This is because the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

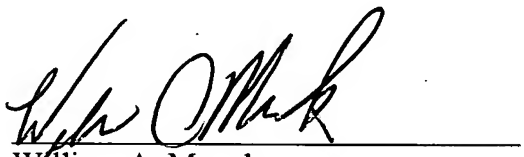
For these reasons, the elements of the *Dai* reference do not anticipate the Appellants' invention as claimed in Claims 1-2, 24-29 and 33-36. Accordingly, the Appellants respectfully request the Board to reverse the outstanding §102 anticipation rejections and to return this application to the Examiner for allowance.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Munck Carter Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, P.C.

Date: 01-12-2009



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| Group No. | : | 2816 |
| Examiner | : | Tuan Thieu Lam |
| Confirmation No. | : | 4869 |

## APPENDIX A -
## Claims Appendix
**37 C.F.R. § 41.37 (c)(1)(viii)**

1. (Previously Presented) A variable phase-shifting circuit comprising:

an input for receiving an input signal having a specified oscillation frequency;

an output for delivering an output signal having said specified oscillation frequency and having a variable phase-shift with respect to said input signal;

at least one control input for receiving a control signal which controls the phase-shift of said output signal with respect to said input signal; and

a synchronized oscillator comprising a synchronization input coupled to said input of the variable phase-shifting circuit and an output coupled to said output of the variable phase-shifting

circuit, said synchronized oscillator having a variable free-running oscillation frequency controlled by said control signal;

wherein the input signal originates from a source that is external to the synchronized oscillator.

2. (Previously Presented) The circuit of Claim 1, wherein the synchronized oscillator further comprises an astable multivibrator circuit having a first branch and a second branch arranged in parallel between a positive supply terminal and a negative supply terminal or ground, and means for delivering into the first branch and into the second branch a respective quiescent current of a same specified value, said quiescent current being controlled by the control signal.

3. (Previously Presented) The circuit of Claim 2, wherein, for each branch, the means for delivering a quiescent current into the branch comprises a respective current source arranged in series in the branch, which delivers a current of a specified value, and wherein the control signal is a current control signal which is added to said current of a specified value.

4. (Previously Withdrawn) Phase interpolator comprising:

- a signal output which delivers an output signal;

- at least one data input receiving a digital input value coded in P bits, where P is an integer, representing the difference between an actual instant of switching of a pulse of a signal to be interpolated and a desired instant of switching said output signal;

- N1 first variable phase-shifting circuits, where N1 is an integer strictly greater than one, each comprising an input which receives an input signal having the frequency of a reference signal, the input signals received by said respective inputs of said N1 variable phase-shifting circuits being respectively phase-shifted by 360°/N1, each variable phase-shifting circuit further comprising a control input receiving a control signal and an output which delivers an output signal corresponding to the signal received at the input phase-shifted based on said control signal, and each variable phase-shifting circuit comprising a synchronized oscillator having at least one synchronization input coupled to said variable phase-shifting circuit input , at least one output coupled to the said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency which is controlled by said control signal;

- a multiplexer having N1 inputs which receive the N1 signals delivered by the respective output of the N1 variable phase-shifting circuits and an output which delivers one of the said N1 signals based on the value of a given number Q of the most significant bits of the digital input value, where Q is an integer less than or equal to P.

5. (Previously Withdrawn) The phase interpolator of Claim 4, further comprising a digital/analog converter having P-Q inputs which receive the P-Q least significant bits of the digital input value, and having an output which delivers, based on the value of said P-Q bits, an analog phase-shift correction signal which is delivered at the control input of at least one of the N1 first variable phase-shifting circuits.

6. (Previously Withdrawn) The phase interpolator of Claim 4 wherein the phase-shift correction signal is delivered at the control input of each of the N1 first variable phase-shifting circuits.

7. (Previously Withdrawn) The phase interpolator of Claim 4 further comprising a demultiplexer having an input receiving the phase-shift correction signal, at least N1 outputs respectively coupled to the control input of the N1 first variable phase-shifting circuits, and directing the phase-shift correction signal to the control input of one of the said N1 first variable phase-shifting circuits based on the value of the Q most significant bits of the digital input value.

8. (Previously Withdrawn) The phase interpolator of Claim 4, further comprising a multiphase clock generator comprising:

- N1 second variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N1 second variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N1 second variable phase-shifting circuits, and an output;

- a low-pass filter with an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N1 first outputs delivering N1 identical first calibration signals respectively, which are applied to the respective control inputs of said N1 second variable phase-shifting circuits.

9. (Previously Withdrawn) The phase interpolator of Claim 8, wherein the adaptation module of the multiphase clock generator further comprises an N1 + 1-th output, delivering an N1 + 1-th calibration signal identical to the calibration signals generated by the N1 first outputs, and coupled to the digital-analog converter.

10. (Previously Withdrawn) The phase interpolator of Claim 4 further comprising calibration means comprising:

- N2 third variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N2 third variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N2 third variable phase-shifting circuits, and an output;

- a low-pass filter having an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N2 + 1 outputs delivering N2 + 1 identical second calibration signals respectively, among which N2 outputs are coupled to the respective control inputs of said N2 third variable phase-shifting circuits.

11. (Previously Withdrawn) The phase interpolator of Claim 10, wherein the adaptation module of the calibration means includes N2 + 1 outputs delivering respectively N2 + 1 identical second calibration signals among which, in addition, the N2 + 1-th output is coupled to the digital-analog converter so as to provide it with a second reference value.

12. (Previously Withdrawn) The phase interpolator of Claim 10, wherein the adaptation module of the calibration means includes N2 + 2xN1 outputs delivering respectively N2 + 2xN1 identical second calibration signals, among which, N1 other outputs are further coupled to the respective control inputs of the N1 second variable phase-shifting circuits of the multiphase clock generator, and among which N1 other outputs are coupled to the respective control inputs of the N1 first variable phase-shifting circuits.

13. (Previously Withdrawn) The phase interpolator of Claim 4, wherein further comprising an input receiving a signal for activating/deactivating the multiplexer, to control the frequency of the output signal with respect to the reference signal frequency.

14. (Previously Withdrawn) Digital frequency synthesizer comprising a phase accumulator and a phase interpolator coupled to said phase accumulator, wherein said phase interpolator comprises:

- a signal output which delivers an output signal;

- at least one data input receiving a digital input value coded in P bits, where P is an integer, representing the difference between an actual instant of switching of a pulse of a signal to be interpolated and a desired instant of switching said output signal;

- N1 first variable phase-shifting circuits, where N1 is an integer strictly greater than one, each comprising an input which receives an input signal having the frequency of a reference signal, the input signals received by said respective inputs of said N1 variable phase-shifting

circuits being respectively phase-shifted by 360°/N1, each variable phase-shifting circuit further comprising a control input receiving a control signal and an output which delivers an output signal corresponding to the signal received at the input phase-shifted based on said control signal, and each variable phase-shifting circuit comprising a synchronized oscillator having at least one synchronization input coupled to said variable phase-shifting circuit input, at least one output coupled to the said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency which is controlled by said control signal;

- a multiplexer having N1 inputs which receive the N1 signals delivered by the respective output of the N1 variable phase-shifting circuits and an output which delivers one of the said N1 signals based on the value of a given number Q of the most significant bits of the digital input value, where Q is an integer less than or equal to P.

15. (Previously Withdrawn) The Digital frequency synthesizer of Claim 14, wherein the phase interpolator, further comprises a digital/analog converter having P-Q inputs which receive the P-Q least significant bits of the digital input value, and having an output which delivers, based on the value of said P-Q bits, an analog phase-shift correction signal which is delivered at the control input of at least one of the N1 first available phase-shifting circuits.

16. (Previously Withdrawn) The Digital frequency synthesizer of Claim 14, wherein the phase-shift correction signal is delivered at the control input of each of the N1 first variable phase-shifting circuits.

17. (Previously Withdrawn) The Digital frequency synthesizer of Claim 14, further comprising a demultiplexer having an input receiving the phase-shift correction signal, at least N1 outputs respectively coupled to the control input of the N1 first variable phase-shifting circuits, and directing the phase-shift correction signal to the control input of one of the said N1 first variable phase-shifting circuits based on the value of the Q most significant bits of the digital input value.

18. (Previously Withdrawn) The Digital frequency synthesize of Claim 14, further comprising a multiphase clock generator comprising:

- N1 second variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N1 second variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N1 second variable phase-shifting circuits; and an output;

- a low-pass filter with an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N1 first outputs delivering N1 identical first calibration signals respectively, which are applied to the respective control inputs of said N1 second variable phase-shifting circuits.

19. (Previously Withdrawn) The Digital frequency synthesizer of Claim 18, wherein the adaptation module of the multiphase clock generator further comprises an N1 + 1-th output, delivering an N1 + 1-th calibration signal identical to the calibration signals generated by the N1 first outputs, and coupled to the digital-analog converter.

20. (Previously Withdrawn) The Digital frequency synthesizer of Claim 14 further comprising calibration means comprising:

- N2 third variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N2 third variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N2 third variable phase-shifting circuits, and an output;

- a low-pass filter having an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N2 + 1 outputs delivering N2 + 1 identical second calibration signals respectively, among

which N2 outputs are coupled to the respective control inputs of said N2 third variable phase-shifting circuits.

21. (Previously Withdrawn) The Digital frequency synthesizer of Claim 20, wherein the adaptation module of the calibration means includes N2 + 1 outputs delivering respectively N2 + 1 identical second calibration signals among which, in addition, the N2 + 1-th output is coupled to the digital-analog converter so as to provide it with a second reference value.

22. (Previously Withdrawn) The Digital frequency synthesizer of Claim 20, wherein the adaptation module of the calibration means includes N2 + 2xN1 outputs delivering respectively N2 + 2xN1 identical second calibration signals, among which, N1 other outputs are further coupled to the respective control inputs of the N1 second variable phase-shifting circuits of the multiphase clock generator, and among which N1 other outputs are coupled to the respective control inputs of the N1 first variable phase-shifting circuits.

23. (Previously Withdrawn) The Digital frequency synthesizer of Claim 14, wherein further comprising an input receiving a signal for activating/deactivating the multiplexer, to control the frequency of the output signal with respect to the reference signal frequency.

24. (Previously Presented) A variable phase-shifting circuit comprising:

an input and an output having a specified oscillation frequency, said output having a variable phase-shift with respect to said input;

a control signal for controlling the phase-shift of said output with respect to said input; and

a synchronized oscillator having a synchronization input coupled to said input of said variable phase-shifting circuit and a second output coupled to said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency controlled by said control signal;

wherein the input of the variable phase-shifting circuit originates from a source that is external to the synchronized oscillator.

25. (Previously Presented) The circuit of Claim 24, wherein said synchronized oscillator further comprises an astable multivibrator circuit.

26. (Previously Presented) The circuit of Claim 25, wherein said astable multivibrator circuit further comprises a first branch and a second branch arranged in parallel between a positive supply terminal and a negative supply terminal or ground of the variable phase-shifting circuit.

27. (Previously Presented) The circuit of Claim 26 further comprising:

a delivery circuit arranged to deliver a respective quiescent current of a same specified value into said first branch and into said second branch.

28. (Previously Presented) The circuit of Claim 27, wherein said quiescent current is controlled by said control signal.

29. (Previously Presented) The circuit of Claim 27, wherein for each branch, said delivery circuit delivers said quiescent current into said branch.

30. (Previously Presented) The circuit of Claim 27, wherein each said branch comprising a respective current source arranged in series in the branch.

31. (Previously Presented) The circuit of Claim 30, wherein said respective current source delivers a current of a specified value.

32. (Previously Presented) The circuit of claim 31, wherein the control signal is a current control signal added to said current of a specified value.

33. (Previously Presented) A variable phase-shifting circuit comprising:

an input and an output having a specified oscillation frequency, said output having a variable phase-shift with respect to said input;

a control signal originating from a source external to said variable phase-shifting circuit to control the phase-shift of said output with respect to said input; and

a synchronized oscillator having a synchronization input coupled to said input of the variable phase-shifting circuit and a second output coupled to said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency controlled by said control signal;

wherein the synchronized oscillator comprises an astable multivibrator circuit having a first branch and a second branch arranged in parallel between a positive supply terminal and a negative supply terminal or ground of said variable phase-shifting circuit.

34. (Previously Presented) The circuit of Claim 33 further comprising:

a delivery circuit arranged to deliver a respective quiescent current of a same specified value into said first branch and into said second branch.

35. (Previously Presented) The circuit of Claim 34, wherein said quiescent current is controlled by said control signal.

36. (Previously Presented) The circuit of Claim 34, wherein for each branch, said delivery circuit delivers said quiescent current into said branch.

37. (Previously Presented) The circuit of Claim 34, wherein each said branch comprising a respective current source arranged in series in the branch.

38. (Previously Presented) The circuit of Claim 37, wherein said respective current source delivers a current of a specified value.

39. (Previously Presented) The circuit of claim 38, wherein the control signal is a current control signal added to said current of a specified value.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Filed | : | June 25, 2003 |
| For | : | VARIABLE PHASE-SHIFTING CIRCUIT, PHASE INTERPOLATOR INCORPORATING IT, AND DIGITAL FREQUENCY SYNTHESIZER INCORPORATING SUCH AN INTERPOLATOR |
| Group No. | : | 2816 |
| Examiner | : | Tuan Thieu Lam |
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# APPENDIX B
## Evidence Appendix
**37 C.F.R. § 41.37 (c)(1)(ix)**

None

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# APPENDIX C
## Related Proceedings Appendix
**37 C.F.R. § 41.37 (c)(1)(x)**

None